Attorney Docket No. 5646-42XX PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Mario Au et al.
Serial No. 10/613,246
Filed: July 3, 2003

Confirmation No. 4741
Group Art Unit: 2188
Examiner: Gary J. Portka

For: **INTEGRATED CIRCUIT MEMORY DEVICES HAVING CLOCK SIGNAL ARBITRATION CIRCUITS THEREIN AND METHODS OF PERFORMING CLOCK SIGNAL ARBITRATION**

April 17, 2006

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1451

AMENDMENT A

Sir:

This response addresses the Official Action of December 16, 2005.

In the Claims:

Claims 1-34 (Canceled).

35. (Original) A signal arbitration method, comprising the steps of:

arbitrating between first and second request signals generated in respective first and second clock domains that are asynchronously timed relative to each other, to obtain first arbitration results that identify a relative queue priority between the first and second request signals; and

transferring the first arbitration results into a third clock domain that is asynchronously timed relative to the first and second clock domains.

36. (Currently amended) ~~The method of Claim 35,~~ A signal arbitration method, comprising the steps of:

arbitrating between first and second request signals generated in respective first and second clock domains that are asynchronously timed relative to each other, to obtain first arbitration results that identify a relative queue priority between the first and second request signals; and

transferring the first arbitration results into a third clock domain that is asynchronously timed relative to the first and second clock domains, **[[**wherein**]]** said transferring step **[[**comprises:**]]** comprising arbitrating the first arbitration results in a third clock domain to obtain second arbitration results that confirm or correct the first arbitration results.

37. (Original) The method of Claim 36, wherein said step of arbitrating the first arbitration results is followed by the step of arbitrating the second arbitration results in the third clock domain to obtain third arbitration results that confirm or correct the second arbitration results.

38. (Original) The method of Claim 35, wherein the first and second request signals are read and write request signals, respectively.

39. (Original) A signal arbitration method, comprising the steps of:

arbitrating between first and second request signals generated in respective first and second clock domains that are asynchronously timed relative to each other, to obtain intermediate arbitration results that identify a relative queue priority between the first and second request signals; and

arbitrating between a third request signal and the intermediate arbitration results in a third clock domain that is asynchronously timed relative to the first and second clock domains, to obtain final arbitration results that identify a relative queue priority between the first, second and third request signals.

40. (Original) The method of Claim 39, wherein the third request signal has a higher request priority relative to the first and second request signals.

41. (Currently amended) ~~The method of Claim 40,~~ A signal arbitration method, comprising the steps of:

arbitrating between first and second request signals generated in respective first and second clock domains that are asynchronously timed relative to each other, to obtain intermediate arbitration results that identify a relative queue priority between the first and second request signals; and

arbitrating between a third request signal and the intermediate arbitration results in a third clock domain that is asynchronously timed relative to the first and second clock domains, to obtain final arbitration results that identify a relative queue priority between the first, second and third request signals;

wherein the third request signal has a higher request priority relative to the first and second request signals; and

wherein the first, second and third request signals are received in a first-then-second-then-third timing sequence; and wherein said step of arbitrating between the first and second request signals is followed by the step of performing operations associated with the first, second and third requests one-at-a-time in a first-then-third-then-second operation sequence.

42. (Currently amended) ~~The method of Claim 40,~~ A signal arbitration method, comprising the steps of:

arbitrating between first and second request signals generated in respective first and second clock domains that are asynchronously timed relative to each other, to obtain intermediate arbitration results that identify a relative queue priority between the first and second request signals; and

arbitrating between a third request signal and the intermediate arbitration results in a third clock domain that is asynchronously timed relative to the first and second clock domains, to obtain final arbitration results that identify a relative queue priority between the first, second and third request signals;

wherein the third request signal has a higher request priority relative to the first and second request signals; and

wherein the first, second and third request signals are received in a second-then-first-then-third timing sequence; and wherein said step of arbitrating between the first and second request signals is followed by the step of performing operations associated with the first, second and third requests one-at-a-time in a second-then-third-then-first operation sequence.

43. (Original) A signal arbitration method, comprising the steps of:

arbitrating between first and second request signals generated in respective first and second clock domains that are asynchronously timed relative to each other, to obtain first arbitration results that identify the first request signal as having a higher queue priority relative to the second request signal;

transferring the first arbitration results into a third clock domain that is asynchronously timed relative to the first and second clock domains;

issuing a first start command corresponding to the first request signal in the third clock domain, while maintaining the second request signal as a queued second request; and

arbitrating between a third request signal and the queued second request to obtain second arbitration results that identify a relative queue priority between the second queued request and the third request signal.

44. (Original) The method of Claim 43, wherein the second arbitration results identify the third request signal as having a higher queue priority relative to the second queued request when said step of arbitrating between a third request signal and the queued second request occurs prior to completion of operations responsive to the first start command.

Claims 45-46 (Canceled).

47. (Original) A signal arbitration device, comprising:

a multi-stage arbitration control circuit that is configured to arbitrate between at least first and second request signals generated in respective first and second clock domains that are asynchronously timed relative to each other and transfer arbitration results that identify a relative queue priority between the first and second request signals into a third clock domain that is asynchronously timed relative to the first and second clock domains.

48. (Currently amended) ~~The device of Claim 47,~~ A signal arbitration device, comprising:

a multi-stage arbitration control circuit that is configured to arbitrate between at least first and second request signals generated in respective first and second clock domains that are asynchronously timed relative to each other and transfer arbitration results that identify a relative queue priority between the first and second request signals into a third clock domain that is asynchronously timed relative to the first and second clock domains, **[[**wherein**]]** said multi-stage arbitration control circuit **[[**comprises:**]]** comprising:

a first arbitration stage that is configured to arbitrate a request priority between the at least first and second request signals and generate first arbitration results that identify a relative queue priority between the at least first and second request signals; and

a second arbitration stage that is configured to buffer and rearbitrate a request priority associated with the first arbitration results.

49. (Original) The device of Claim 48, wherein said second arbitration stage is responsive to a clock signal that operates in the third clock domain.

50. (Original) The device of Claim 48, wherein said multi-stage arbitration control circuit is configured to double buffer the first arbitration results.

51. (Original) The device of Claim 50, wherein said second arbitration stage is configured to generate second arbitration results that confirm or correct the first arbitration results.

52. (Original) The device of Claim 51, wherein said multi-stage arbitration control circuit further comprises:

a third arbitration stage that is configured to buffer and rearbitrate a request priority associated with the second arbitration results.

53. (Original) The device of Claim 52, wherein said third arbitration stage is electrically coupled to a clock control circuit that is responsive to the third arbitration results.

54. (Original) The device of Claim 53, wherein the clock control circuit is responsive to the clock signal that operates in the third clock domain.

55. (Currently amended) A signal arbitration device, comprising:

a multi-stage arbitration control circuit that is configured to arbitrate between read and write request signals generated in respective first and second clock domains that are asynchronously timed relative to each other and is further configured to transfer arbitration results that identify a relative queue priority between the read and write request signals into a third clock domain that is asynchronously timed relative to the first and second clock domains; and

a refresh command buffer and arbitration circuit that is responsive to a refresh start command and read and write start signals generated by said multi-stage arbitration control circuit.

56. (Original) The device of Claim 55, further comprising a clock control circuit that is responsive to read, write and refresh start signals generated by said multi-stage arbitration control circuit and said refresh command buffer and arbitration circuit.

57. (Original) The device of Claim 56, wherein said multi-stage arbitration control circuit is responsive to a clock signal generated by said clock control circuit.

58. (Original) The device of Claim 57, wherein said multi-stage arbitration control circuit comprises a third stage that is synchronized with the clock signal generated by said clock control circuit.

Claim 59 (Canceled).

REMARKS

Applicants appreciate the examination of the application that is evidenced by the Official Action of December 16, 2005 and affirm the prior election of the Group I invention, which has now resulted in the cancellation of Claims 45-46. In response to the Official Action, Applicants have rewritten Claims 36, 41-42 and 48 in independent form. A typographical error in independent Claim 55 has also been corrected to address the section 112 rejection of Claims 55-58. Because it does not appear that any rejections are outstanding with respect to Claims 48-54, Applicants respectfully submit that Claims 48-54 are now in condition for allowance. Applicants will now address the remaining rejections based on sections 102 and 112.

Claims 36-37 and 39-42 Meet the Requirements of Section 112

Applicants respectfully submit that the concept of arbitrating more than once between competing requests is properly recited by the identified claims and sufficiently explained with respect to the arbitration circuit **500** of FIG. 17A, which includes multiple arbitration stages (shown as 1st Stage **508**, 2nd Stage **510** and 3rd Stage **512**). For example, at page 44 of the present application, the "second stage" arbitration circuit **510** is described as being "configured to buffer and rearbitrate the first arbitration results (RSTART1 and WSTART1) and generate second arbitration results (RSTART2 and WSTART2). These second arbitration results "confirm or, if necessary, correct the first arbitration results if timing jitter caused an erroneous initial result." (See, page 44, lines 26-30). As further described at page 45 of the application, the second arbitration results "represent a transfer of the first arbitration results into a new clock domain ... that is asynchronously timed relative to the clock domains associated with the generation of the read and write request signals ...."

Accordingly, Applicants respectfully submit that it is not unclear what it means to arbitrate previously generated "arbitration results" – where the "rearbitration" represents a form of "buffering" of prior arbitration results to confirm their accuracy or correct an inaccuracy caused by timing jitter. Based on these

remarks, Applicants respectfully submit that Claims 36-37 and 41-42, which have only been rejected under section 112, are in condition for allowance.

Claims 35, 38-40, 43-44, 47 and 55-58 are Patentable Over Niu et al.

Applicants acknowledge that FIG. 2 of Niu (US 6,161,160) discloses the use of a network interface device **10** that operates in two distinct clock domains **56a** and **56b**, which are asynchronously timed relative to each other. (See, Niu, Col. 7, lines 36-38). The host computer bus clock domain **56a** in FIG. 2 operates in-sync with a PCI bus clock (BCLK), which synchronizes both transmit and receive operations on buses **62b** and **62a**, respectively. In contrast, the network clock domain **56b** in FIG. 2 operates in-sync with a MAC receive clock (RX_CLK) on one bus and a MAC transmit clock (TX_CLK) on another bus. Thus, Niu shows two clocks in one domain **56b** and one clock in the other domain **56a**.

Applicants respectfully submit, however, that Niu does not disclose or suggest the claimed invention as argued by the Examiner. As described with respect to FIG. 2 of Niu, each of the management blocks **22a**, **22b**, **22c** and **22d** operate as event-driven controllers that transfer data in response to detected conditions by the synchronization circuit **60**. (See, Niu, Col. 12, lines 9-16). To achieve this "event-driven" operation, the asynchronous monitors **82a** and **82b** in FIG. 4 monitor the amount of receive data and the amount of transmit data stored in the SRAMs **18a** and **18b**, respectively. This monitoring, which is entirely event-driven based on a whether a full data frame **64** is stored in an SRAM memory (**18a** or **18b**), eliminates all clock contention between the distinct clock domains (i.e., eliminates need to arbitrate between requests that are synchronized with different clocks):

> "Hence, the synchronization circuit can asynchronously determine the presence of at least one stored data frame in either the RX SRAM **18a** or the TX SRAM **18b**, independent of the clock domains used to write and read into the respective transmit or receive buffers." (See, Niu, Col. 11, lines 23-27).

Thus, as described throughout Niu, the complex problem of arbitrating between signals (e.g., read and write requests) that are generated in distinct clock domains can be eliminated by making the read and write transfers from the memory devices (i.e., RX SRAM **18a** or TX SRAM **18b**) a function of when these memory devices are filled to the point of storing a full data frame. In this manner, each of the management blocks **22a**, **22b**, **22c** and **22d** in Niu can operate in its respective clock domain, without regard to the operations of other management blocks in other clock domains. (See, Niu, Col 12, lines 16-21).

This simplified "event-driven" management in Niu, which eliminates contention between clock signals in different domains, is in stark contrast to the operations required to establish queue priority between competing requests (read, write, refresh), as recited by the claims of the present application. (See, e.g., FIGS. 15A-15D and 16A-16H of the present application). For example, independent Claim 35 recites "obtaining first arbitration results that identify a relative queue priority between ... first and second request signals" generated in different clock domains. Niu provides absolutely no disclosure or suggestion of identifying any relative queue priorities based on signal arbitration. Instead, the "event-driven" management in Niu is "independent of the clock domains used to write and read into the respective transmit or receive buffers." (Niu, Col. 11, lines 25-27).

These same arguments apply equally to the remaining independent Claims 39, 43, 47 and 55, which all contain recitations relating to the identification of a queue priority based on signal arbitration.

Based on these arguments, Applicants respectfully submit that all pending claims are in condition for allowance, which is respectfully requested.

Respectfully submitted,

Grant J. Scott
Registration No. 36,925

USPTO Customer No. 20792
Myers Bigel Sibley & Sajovec
Post Office Box 37428
Raleigh, North Carolina 27627
Telephone: 919/854-1400
Facsimile: 919/854-1401

CERTIFICATION OF ELECTRONIC TRANSMISSION

I hereby certify that this correspondence is being transmitted electronically to the U.S. Patent and Trademark Office on April 17, 2006.

Candi L. Riggs

#479249